WHAT IS CLAIMED IS:

1. A semiconductor device comprising a first interconnect pattern, a first dielectric film covering top and side surfaces of said first interconnect pattern and having therein through-holes, a second interconnect pattern electrically connected to said first interconnect pattern via said through-holes, a semiconductor chip having a plurality of chip electrodes and mounted on said first dielectric film, interconnect members for connecting said chip electrodes to said second interconnect patterns, an encapsulating resin for encapsulating said semiconductor chip and said interconnect members on said first dielectric film, and a second dielectric film covering a bottom surface of said first interconnect pattern.

2. A semiconductor device as defined in claim 1, further comprising a plurality of external terminals formed on said bottom surface of said first interconnect pattern and exposed from said second dielectric film.

3. The semiconductor device as defined in claim 2, wherein said external terminals are metallic bumps.

4. The semiconductor device as defined in claim 1, wherein portions of said first interconnect pattern are formed as a plurality of external terminals.

5. The semiconductor device as defined in claim 1, wherein said interconnect members are metallic bumps.

6. The semiconductor device as defined in claim 1, wherein said interconnect members are bonding wires.

7. A method for fabricating a semiconductor device comprising the steps of forming a first interconnect pattern on a metallic plate, forming a first dielectric film having a plurality of through-holes on said first interconnect pattern, forming a second interconnect pattern on said first dielectric film, said second interconnect pattern being electrically connected to said first interconnect pattern via said through-holes, mounting a semiconductor chip having a plurality of chip electrodes on said first dielectric film, connecting said chip electrodes to said second interconnect pattern, encapsulating said semiconductor chip on said first dielectric film, removing said metallic plate at a bottom surface thereof selectively from said first interconnect pattern, and forming a second dielectric film on a bottom surface said first interconnect pattern.

8. The method as defined in claim 7, further comprising the steps of forming a plurality of external terminals on said first interconnect pattern.

9. The method as defined in claim 7, wherein said first interconnect pattern is formed by etching said metallic plate.

10. The method as defined in claim 9, wherein said etching is implemented by one of chemical etching, chemical mechanical etching, mechanical grinding and mechanical peeling-off.

11. The method as defined in claim 7, wherein said second dielectric film is an adhesive sheet.

12. A method for fabricating a semiconductor device comprising the steps of forming a first interconnect pattern on a top surface of metallic plate, forming a second interconnect pattern on a bottom surface of a metallic plate, mounting a semiconductor chip having a plurality of chip electrodes on said top surface of said metallic plate, connecting said chip electrodes to said first interconnect pattern, encapsulating said semiconductor chip on said top surface of said metallic plate, removing said metallic plate by using said second interconnect pattern as a mask, forming a plurality of external electrodes on said second interconnect pattern, and forming a dielectric film on said second interconnect pattern and an area from which said metallic plate is removed, said dielectric film exposing therefrom said external electrodes.

13. The method as defined in claim 12, wherein said connecting

step uses metallic bumps or bonding wires.

14. The method as defined in claim 12, wherein said first interconnect pattern is formed by plating.

15. The method as defined in claim 12, wherein said metallic plate is a Cu plate and said second interconnect pattern is formed by plating.